AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

1) Page 8, line 20 – page 9, line 11:

"Reference is once again made to **Figure 2**, wherein control interface **105** is shown. In addition to the logic described above, control interface **105** further includes write cycle decode logic **112** and read cycle decode logic **114**. Write cycle decode logic **112** receives read/write control signals **124** as input, and outputs write control signal **125** to IC **100** based upon the operational mode specified by mode control signal **130**. For example, if mode control signal **130** indicates one mode of operation, write cycle decode logic **112** will output a write control indication on write control line **125** when both a transfer start indication and a write indication are present on read/write control bus **124**. Similarly, if mode control signal **130** indicates another mode of operation, write cycle decode will output a write control indication on write control line **125** when a mere write strobe is present. The read cycle decode logic receives read/write control signals **124** as input, and outputs read control signal **127** to IC **100** also based upon the operational mode specified by mode control signal **130**. For example, if mode control signal **130** indicates a first mode of operation, read cycle decode will output a read control indication on read control line **127** when both a transfer start indication and a read indication are present on read/write control bus **124**. Similarly, if mode control signal **130** indicates a second mode of operation, read cycle decode will output a read control indication on read control line **127** when a mere read strobe is present."

2) Page 10, lines 4-16:

"In one embodiment of the invention, mode control signal **130** represents two control signals enabling four independently programmable operating modes for control interface **105**. For example, a first control signal is used to select between a first operating mode whereby multiplexed address and data signals are received on host address/data bus **120**, and a second operating mode whereby ~~addresses are~~data is received on host address/data bus **120** and ~~data~~ address signals are received on separate host address bus **122**. Similarly, a second control signal is used to select between a third operating mode whereby a transfer start indication is used in

cooperation with a read/write indication to signify the start of either a read or a write transaction, and a fourth operating mode whereby separate read and write strobes are used to signal the start of a read/write transaction. In accordance with one embodiment of the invention, each mode control signal may be independently set or cleared based upon the architecture of processor **102**."

3) Page 10, line 18 – page 11, line 5:

"**Figure 4** is a block diagram illustrating two operating modes for control interface **105**, in accordance with one embodiment. The components depicted in **Figure 4** are functionally identical to their analogues of **Figure 2**, but have been redrawn for the purpose of clarity. In **Figure 4**, three signal paths have additionally been indicated by the encircled labels of (**1**), (**2**), and (**3**). In accordance with the teachings of the present invention, signal paths (**1**) and (**2**) together indicate signal paths that would be followed by data and addresses received from a processor utilizing a multiplexed address and data bus, assuming MUX **110** (and by extension control interface **105**) is set via mode control signal ~~**130**~~ **130a** to operate in a first operational mode. Signal paths (**1**) and (**3**) indicate signal paths that would be followed by data and addresses received from a processor utilizing separate data and address buses, assuming MUX **110** is set via mode control signal ~~**130**~~ **130a** to operate in a second operational mode, for example. Accordingly, MUX **110** selects between two signal paths (e.g., (**2**) and (**3**)) based at least in part upon the architecture of the host processor."

4) Page 12, lines 5-18:

"**Figures 6A-D** represent timing diagrams illustrating the various read and write cycle signaling of the host side of control interface **105**, in accordance with various operational modes. **Figure 6A** is a timing diagram illustrating the operation of control interface **105** in accordance with a first operating mode where separate address and data bus is used in conjunction with transfer start and read/write signaling. **Figure 6B** is a timing diagram illustrating the operation of control interface **105** in accordance with a second operating mode where a multiplexed address and data bus is used in conjunction with transfer start and read/write signaling. **Figure 6C** is a timing diagram

illustrating the operation of control interface **105** in accordance with a ~~first~~ third operating mode where separate address and data bus is used in conjunction with read/write strobes. **Figure 6D** is a timing diagram illustrating the operation of control interface **105** in accordance with a ~~second~~ fourth operating mode where a multiplexed address and data bus is used in conjunction with read/write strobes."